

100GHz S-Parameter Measurements of Monolithically Integrated Silicon Impatt Diodes

C. Schöllhorn*, W. Zhao*, M. Morschbach*, M. Oehme*, E. Kasper*, J. Hasch⁺ and H. Irion⁺

* : Institut für Halbleitertechnik, Universität Stuttgart, Pfaffenwaldring 47, 70569 Stuttgart, Germany

⁺ : Bosch Company Research Department FV/FLO, Schillerhöhe, 70049 Stuttgart, Germany

Corresponding Author : Claus Schöllhorn, phone : +49 711 685 8007; fax : +49 711 685 8044; e-mail : schoellhorn@iht.uni-stuttgart.de

Abstract Silicon based monolithic Impatt diodes are investigated. The Impatt diodes are integrated in coplanar waveguides with aluminum metallization. S-parameter measurements are performed from 75 GHz up to 110 GHz measuring the reflection coefficient S_{11} . The diodes show a negative real- and imaginary part of the impedance.

Keywords : coplanar waveguides, silicon Impatt diodes, S-parameter measurements

1. Introduction

Silicon based Impatt diodes are used as discrete sources of mm-wave oscillators [1]. Normally they are mounted on special heat sinks to reduce the operating temperature. In contrast to this we investigated in monolithically integrated Impatt diodes, fabricated with processes very close to standard CMOS processes. The layer stack of these diodes was designed for avalanche frequencies between 60GHz and 100GHz. In interaction with a matching resonator, oscillations above this frequency are possible. The structures were grown with molecular beam epitaxy (MBE) in a special low temperature process to achieve very sharp doping profiles. For a future integration with varactor or schottky diodes we realized a single drift (SD) profile. This enables the realization of tunable planar oscillators. To perform RF measurements the diodes are integrated into coplanar waveguides (CPW) as part of silicon monolithic millimeter-wave integrated circuits (SIMMWICs).

2. Technology

Because the attenuation depends on the resistivity of the substrate we used a float zone (FZ) silicon substrate with specific resistance $\rho > 1000 \Omega \text{cm}$. The growth of the complete device sequence starts with the highly doped boron buried layer. The doping level is $1 \text{e}20 \text{cm}^{-3}$ and the thickness is 350nm.

Thereafter the combined avalanche/drift region is grown with a special growth technology to guarantee the sharp doping profile over 4 decades and a constant doping level : at the beginning of the growth of the avalanche/drift region a 0.1 monolayer of antimony is deposited at the surface. At a growth temperature of

650°C this adlayer is incorporated. This leads to a doping level of $2.2 \text{e}17 \text{cm}^{-3}$. The dependency of the doping level from the temperature and the Si growth rate are described in more detail in [2]. At last the upper contact layer is grown. It's thickness is 200nm and the antimony doping level is $3 \text{e}20 \text{cm}^{-3}$. Fig. 1 shows the layer stack and a cross section of a processed diode. To realize the planar diodes the following steps are performed :

- The first step is a mesa etch step which is used to make the contact to the high doped buried layer. This step is a dry etching step which causes only a very small damage in the buried layer, leading to very small contact resistances usually smaller than $1.8 \text{exp}-6 \Omega/\text{cm}^2$.
- The second step is a trench etching step, which isolates the buried layer of the diodes. Besides this the high doped silicon outlying of the active area is removed, to reduce the attenuation of the coplanar waveguides.
- After the deposition of the isolating oxide the patterning and etching of the contact holes is performed. This oxide is a low temperature PECVD-(plasma enhanced chemical vapor deposition)-oxide grown at 350°C to avoid any smearing of the doping profiles.
- The last step is the sputtering and patterning of the aluminum layer with a thickness of $1 \mu\text{m}$.

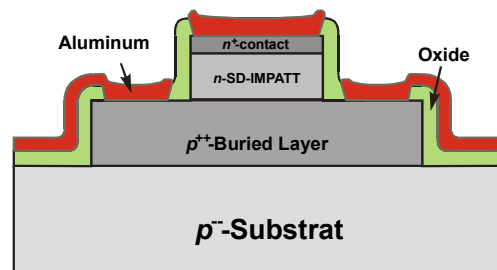


Fig. 1 Layer stack and cross section of a processed Impatt diode

Fig. 2 shows a scanning electron microscope (SEM) picture of a realized integrated Impatt diode.

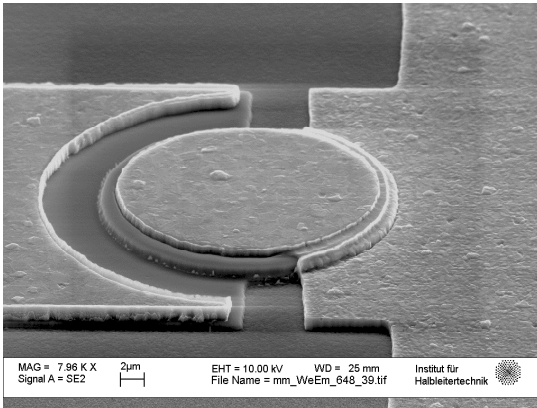


Fig. 2 SEM picture of a monolithically integrated Impatt diode with aluminum metallization

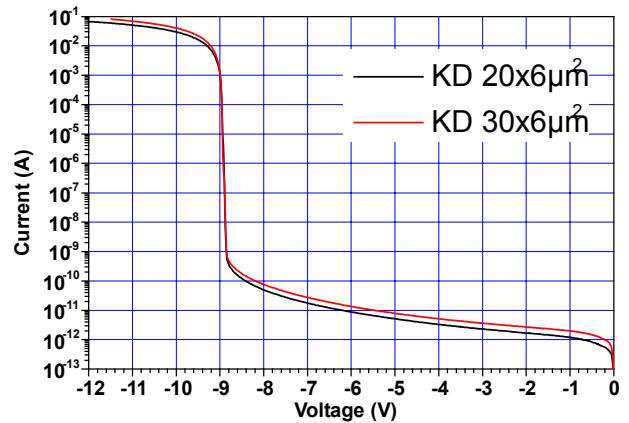


Fig. 4 Backward current and break-through of an Impatt diode

3. Direct current (DC) measurements

In a first step DC measurements were performed to proof the quality of the MBE layers and the process steps. For Impatt diodes CV measurements are of special interest, to control the doping level and the length of the avalanche/drift region, and the break-through behavior. For CV measurements the diode is assumed to be a plate capacitor with the length of the space charge region being the distance of the plates. This length depends on the applied voltage if it is reverse biased and the resulting capacitance depends on the doping level [3]. The results of the CV measurements are shown in fig. 3. The achieved doping level reaches the expected level of $2\text{-}3 \times 10^{17} \text{cm}^{-3}$. Fig. 4 shows the backward current of the same sample. Because Impatt diodes are operated in the break-through it is very important to have a reproduceable well defined break-through. The curves show a break-through voltage of -8.8V and a reverse current of $I_b < 4 \times 10^{-12}\text{A}$ for a reverse voltage of $V_b = -1\text{V}$.

4. Radio frequency (RF) measurements

To enable on-wafer S-parameter measurements the Impatt diodes were integrated into coplanar waveguides. The waveguides are designed to have a characteristic impedance of 50Ω . Fig. 5 shows a photograph of the measurement setup, with the coplanar Impatt diode parallel to signal and ground line, and the ground-signal-ground (GSG) probe head.

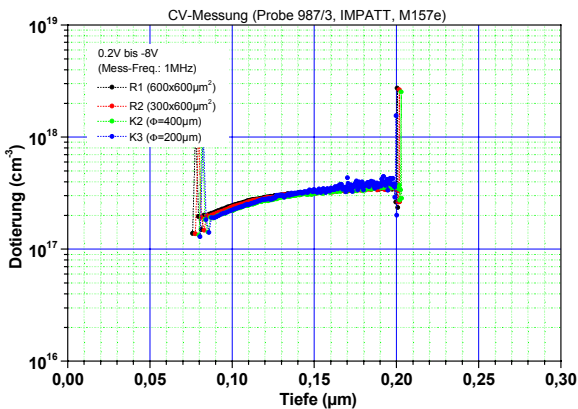


Fig. 3 CV measurement of the diodes to estimate the doping profile

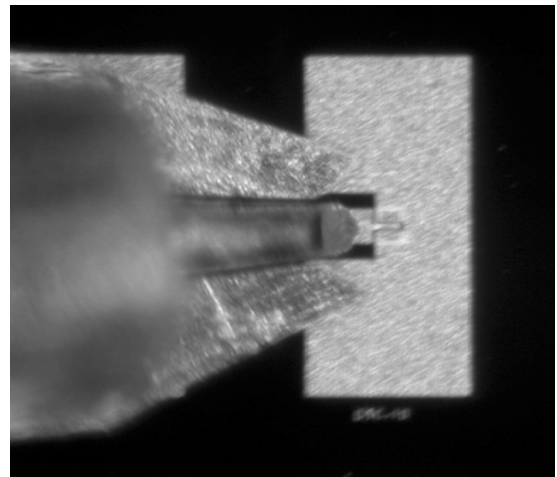


Fig. 5 Photo of the integrated Impatt diode and the RF proper head

By measuring the reflection coefficient, S_{11} , of the Impatt diodes it is possible to estimate the real- and the imaginary part of the impedance of the diodes. The measurements were performed at frequencies from 75GHz up to 110GHz . Fig. 6 and 7 show the smith chart and the real and imaginary part of the impedance.

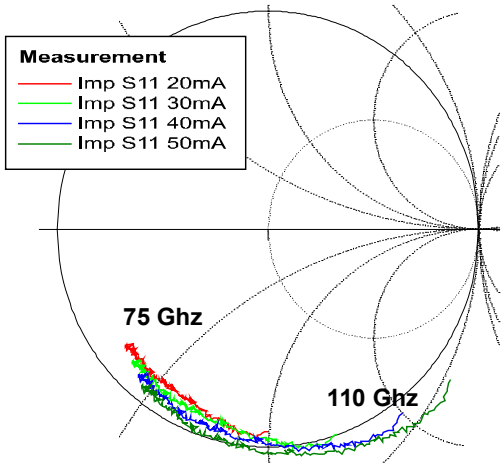


Fig. 6 Smith Chart of the reflection coefficient S_{11} (impedance) of a Impatt diode. Measurement frequency : 75 -110 GHz.

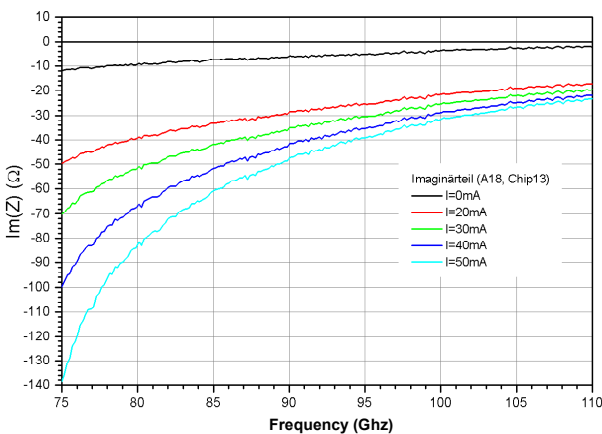
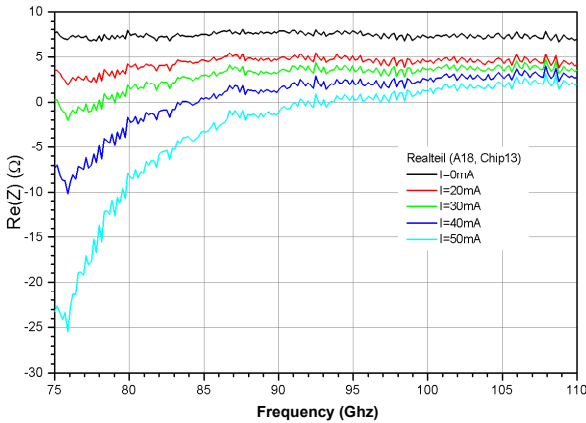


Fig. 7 Real and imaginary part of the processed diode (Frequency range : 75 - 110 GHz).

Because the avalanche frequency depends on the square root of the current density [4], it is possible to increase the avalanche frequency with increasing current. This leads to avalanche frequencies between 58GHz and 70GHz for a current density increasing from $0.167\text{mA}/\mu\text{m}^2$ to $0.417\text{mA}/\mu\text{m}^2$. Because the measurements start at 75GHz the avalanche frequencies were estimated by simulations [5].

5. Conclusion

The results show the possibility to perform S-parameter measurements at Impatt diodes at very high frequencies. The realized diodes have avalanche frequencies between 58GHz and 70GHz. This enables oscillations in the frequency range very close to 100GHz. The negative resistances are high enough to equate the impedance of planar resonators. The realized monolithic integration without heat sinks utilizes process steps of the standard CMOS technology, allowing a cheap and effective process. The next step is the integration of the diodes into the planar resonators.

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