

# Patch Antenna on Micromachined Silicon

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**Abstract** — A rectangular microstrip patch antenna realized as silicon based monolithic millimeter-wave integrated circuit (SIMMWIC) is presented. The antenna was designed for an operating frequency of 122 GHz and manufactured on micromachined high resistivity silicon on insulator (SOI) substrate. Since direct measurements of the far field pattern of an integrated antenna element are difficult at this frequency, a scaled version of the antenna was also manufactured. Far field measurements were performed, to determine the antenna performance and compare with numerical results.

## I. INTRODUCTION

Monolithic integration of a complete millimeter wave frontend on silicon is much desired. This way low cost sensor devices, operating in the millimeter wave range can be achieved [1]. One key element of such an integration effort is the antenna. The integration of the antenna element promises a much simpler packaging, as all millimeter wave signals remain on the silicon chip and do not have to be passed on to an external off-chip substrate, using millimeter wave capable transitions.

There have been a number of publications researching integrated antennas, like [2] or more recently [3]. The technology we have chosen to realize an integrated antenna element has been described in [4]. It is based on silicon bulk micromachining, in order to create a thin silicon membrane. This thin membrane can be used to realize microstrip circuits, in this case a half wavelength rectangular patch antenna.

Micromachining technology was selected, because it offers reliable manufacturing with small tolerances and favorable manufacturing costs. Silicon bulk micromachining is already deployed at a large scale for a number of sensor circuits in production [5].

## II. MICROMACHINING

Because of the high permittivity of silicon, a microstrip patch antenna requires a very small substrate thickness. The influence of substrate thickness and high permittivity substrates on the performance on patch antennas has been examined a number of times, e.g. in [6]. Although an electrically thick substrate improves the antenna bandwidth, it can also excite surface waves, leading to a low radiation efficiency. Surface waves propagate along the substrate and can be reflected back or radiated at the edges of the substrate, leading to a poor antenna pattern.

The fundamental surface wave mode is the  $TM_0$  mode, which has a zero cutoff frequency. The cutoff frequency for higher order  $TE_n$  or  $TM_n$  modes is given in [6]:

$$f_c = \frac{nc}{4d\sqrt{\epsilon_r - 1}}$$

This yields in a substrate thickness of less than 200  $\mu\text{m}$  for silicon at a frequency of 122 GHz, in order to suppress higher surface wave modes. Also coupling of lower surface wave modes becomes stronger with increasing substrate thickness.

Handling a silicon wafer having a thickness of less than 200  $\mu\text{m}$  can be quite difficult, because the wafer becomes very fragile. Our proposed approach is to use a SOI wafer with a thickness of 450  $\mu\text{m}$  and a buried oxide layer (BOX) that separates two silicon layers. The top silicon layer is 50  $\mu\text{m}$  thick and is available with very small thickness tolerances. Typically, the tolerance is below 10 percent or 5  $\mu\text{m}$  for the 50  $\mu\text{m}$  sheet.

Using bulk micromachining, only the part of the wafer where the antenna element is placed will be etched away, forming a 50  $\mu\text{m}$  thick membrane. The rest of the wafer will keep its original thickness of 450  $\mu\text{m}$ . Therefore, the overall stability of the wafer can be retained.

Figure 1 shows a schematic cross section view of such a micromachined wafer.

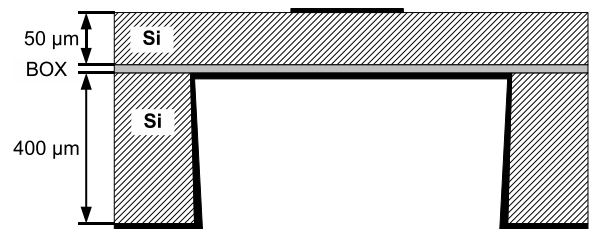


Fig. 1: Schematic cross section view of a micromachined wafer with additional backside metallization.

The backside micromachining is performed utilizing the so called *Bosch Process*, a high performance anisotropic plasma etch process [5]. The thin silicon oxide layer in between the two silicon layers acts as an etch stop, so after the etching step only the bottom silicon layer has been removed. After etching, the wafer backside is metallized by sputtering an aluminum layer with a thickness of a few microns. The patch antenna structure on the top side is created by structuring aluminum with a thickness of 1  $\mu\text{m}$ .

## III. ANTENNA DESIGN

The rectangular microstrip patch was designed using a standard design procedure given in [7]. For excitation, a center microstrip feedline was used, with additional slots for impedance matching. Using a relative permittivity of 11.7 for Silicon and a substrate thickness of 50  $\mu\text{m}$ , the antenna dimensions were calculated to a resonant length  $l = 348 \mu\text{m}$  and  $w = 488 \mu\text{m}$  (see figure 2). The matching slots were calculated having a length of  $s = 138 \mu\text{m}$ .

The microstrip feedline is 42  $\mu\text{m}$  wide, corresponding to

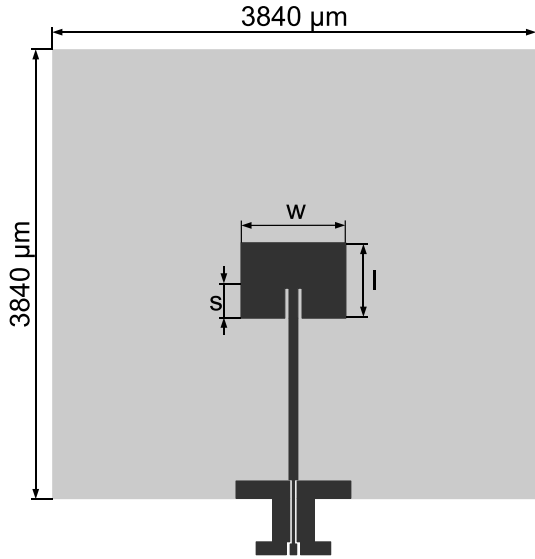


Fig. 2: Top view on micromachined patch antenna layout

a  $50 \Omega$  line and extends to the outer edge of the micromachined area. An onwafer probe tip can be used to contact the antenna, using a coplanar to microstrip transition which extends to the thick silicon area. The transition has been described in more detail in [4]. The contact pads are placed on the thick part of the wafer, so a probe tip can safely contact the antenna without damaging the thin silicon membrane.

The layout of the patch antenna is shown in figure 2. The light grey area shows the extent of the thin micromachined membrane.

#### IV. ANTENNA PERFORMANCE

Using the 3D fullwave simulation program *Microwave Studio*, the antenna characteristics have been computed. Figure 3 shows the simulation results of the input match and the measured data from the fabricated patch antenna. A

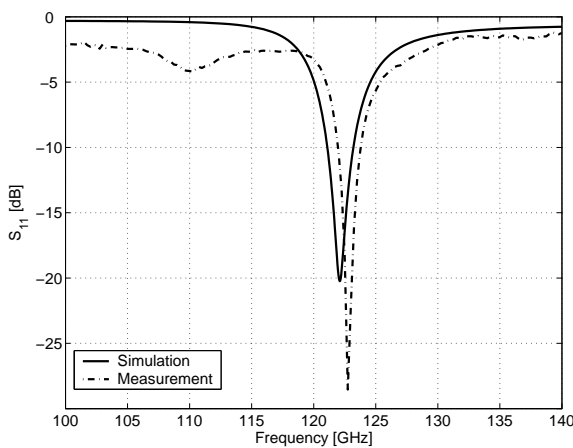


Fig. 3: Reflection coefficient  $|S_{11}|$  of the simulated and measured antenna

match of better than -20 dB is observed, with a -10 dB bandwidth of more than 2 GHz. The slightly different resonance frequencies are due to the buried oxide layer (BOX), which has been neglected in the simulations.

In the computer simulation, the farfield patterns have

also been computed, assuming a finite micromachined area as shown in figure 2. The thick silicon substrate is set to infinite, so only a 180 degree radiation pattern has been computed.

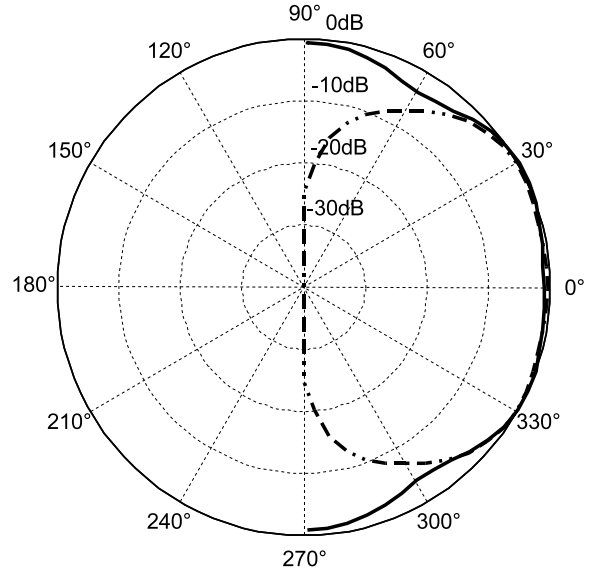


Fig. 4: E-plane (solid) and H-plane (dashed) of the simulated patch antenna farfield pattern at 122 GHz

The 3 dB angles are about 100 degrees in the E- and H-plane. The dents in the E-plane at 90 and 270 degrees are due to surface waves. The simulated antenna shows a gain of 3.2 dBi. Although the antenna is quite narrow band, a -10 dB input reflection bandwidth of more than 2 GHz is sufficient for the 122 GHz frequency band.

#### V. SCALED MODEL

Measuring the farfield radiation pattern of an integrated antenna on silicon is difficult at 122 GHz. If there are no active components integrated on the chip, a low loss millimeter wave signal transition is needed, to get the antenna signal off the chip. The required millimeter wave signal transition is supposed not to radiate itself and not to influence the antenna pattern measurements. This is hard to achieve for an antenna geometry of only a few hundred microns.

An alternative is to build a scaled-size model of the antenna at a lower operating frequency, where the antenna can be connected more easily. Applying the scaling principle leads to the following relations [7]:

Parameter	Description
$l' = n \cdot l$	Geometrical Dimension
$f' = f/n$	Frequency
$\sigma' = \sigma/n$	Conductivity
$\epsilon' = \epsilon$	Permittivity
$Z' = Z$	Input Impedance
$G'_0 = G_0$	Gain

Table 1: Relations between the scaled and nonscaled parameters

According to table 1, all geometrical dimensions are scaled by a factor  $n$ . Using a standard silicon wafer for manufacturing the scaled model, the scaling factor was set to  $n = 12.5$ . This leads to a new silicon substrate thickness of  $625 \mu\text{m}$  and antenna dimensions of  $l = 4850 \mu\text{m}$ ,  $w = 6100 \mu\text{m}$  and  $s = 1725 \mu\text{m}$ . The silicon substrate size is  $48 \times 48 \text{ mm}$ .

Because of the available process technology, the aluminum conductor thickness and conductivity could not be scaled and remain unchanged. Also, the silicon substrate has the same electrical properties, i.e. the permittivity and resistivity remain unchanged.

The silicon wafer was cut and mounted on a metal plate. A coaxial SMA connector was attached to the plate with its inner conductor bonded to the antenna feedline. Figure 5 shows a photo of the antenna setup.

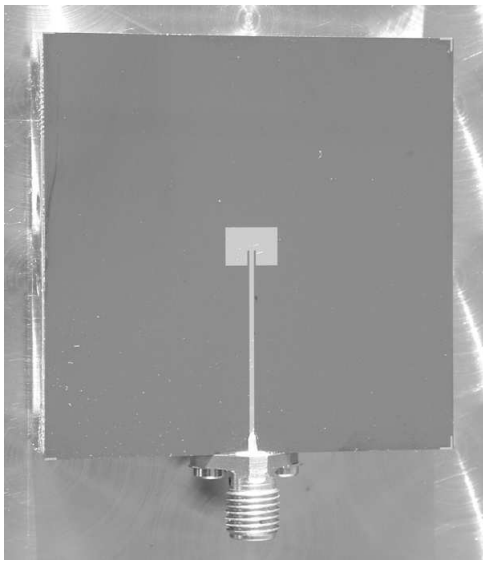


Fig. 5: Photo of the scaled antenna with a SMA connector

The resonant frequency of the scaled model is determined to be at about  $9.6 \text{ GHz}$ . Figure 6 shows the input match of the scaled antenna.

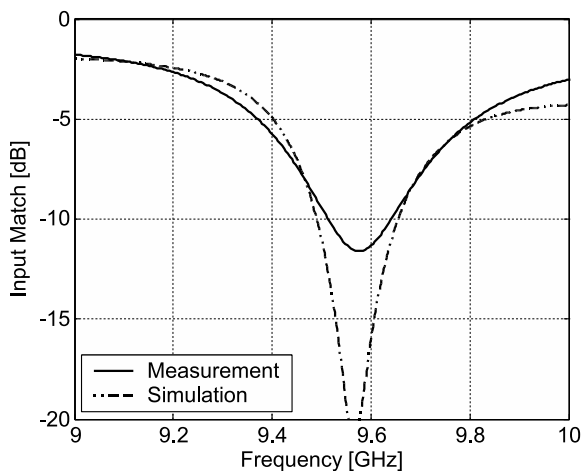


Fig. 6: Measured and simulated input match of the scaled antenna

For the scaled antenna, farfield pattern measurements

have been performed. A comparison between measured and simulated patterns in the E- and H-plane is shown in the figures 7 and 8.

The antenna gain was computed to be  $3.7 \text{ dBi}$ . The measured antenna gain was  $3.6 \text{ dBi}$ , with a measurement uncertainty of  $0.5 \text{ dB}$ .

The influence of the antenna feed can be seen in a dent in the E-plane. The ripples in the antenna pattern are partly due to surface waves.

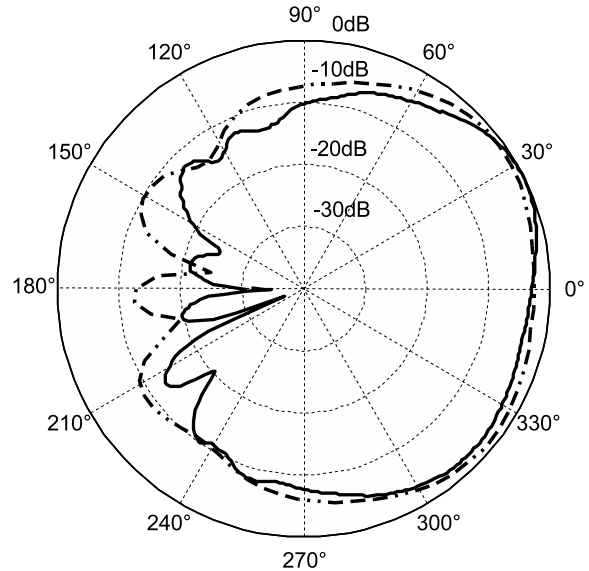


Fig. 7: Measured (solid) and simulated (dashed) E-plane farfield pattern of the scaled patch antenna

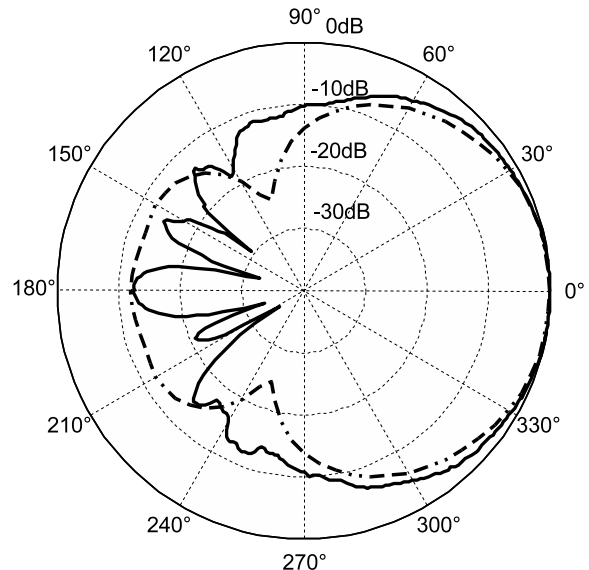


Fig. 8: Measured (solid) and simulated (dashed) H-plane farfield pattern of the scaled patch antenna

## VI. LOSSES

To study the antenna losses, it is convenient to make use of the antenna efficiency. It is defined as the ratio between

the radiated power  $P_{rad}$  and the total input power  $P_{in}$ :

$$\eta = \frac{P_{rad}}{P_{in}}$$

The total efficiency can be split into several parts:

$$\eta = \eta_r \cdot \eta_d \cdot \eta_c \cdot \eta_s$$

- $\eta_r$  - Impedance mismatch. Neglected in the following section, because the impedance match is better than -20 dB for all simulations. This yields a value of  $\eta_r > 0.99$ .
- $\eta_c$  - Conductor losses, caused by the finite conductivity of the metal conductor.
- $\eta_d$  - Dielectric losses, caused by the dielectric loss factor of silicon.
- $\eta_s$  - Surface wave losses, caused by the excitation of substrate surface waves, that do not contribute to the antenna radiation.

Simulations using the method of moments have been carried out to calculate the losses and differentiate between the different loss factors.

Figure 9 shows the effect that the substrate thickness has on the efficiency of a patch antenna, due to surface waves [8]. Numerical simulations for the micromachined patch antenna confirm these values.

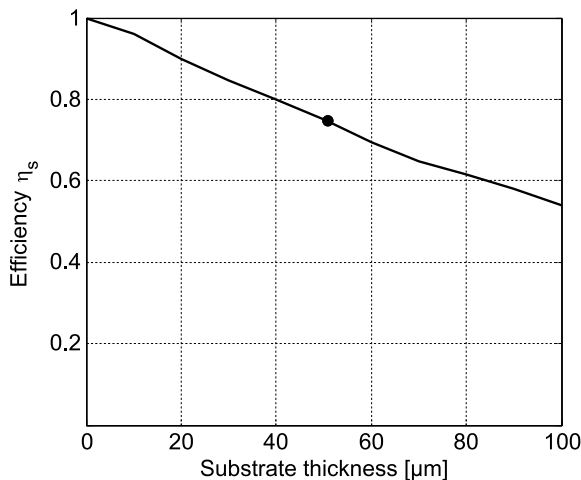


Fig. 9: Antenna efficiency due to surface waves  $\eta_s$  as a function of substrate thickness at 122 GHz

To calculate the conductor losses, an aluminum conductor thickness of  $t = 1 \mu\text{m}$  and a conductivity of  $\sigma = 38 \cdot 10^6 \text{ S/m}$  is assumed. The dielectric losses of the high resistivity silicon wafer are specified by the bulk resistivity of  $\rho = 1000 \Omega\text{cm}$ . For the micromachined antenna at 122 GHz, the individual efficiencies have been computed to  $\eta_d = 0.93$ ,  $\eta_c = 0.75$  and  $\eta_s = 0.74$ . This leads to an overall efficiency of roughly 50 % ( $\eta = 0.52$ ). From these numbers it can be seen, that the surface wave losses and the conductor losses are the major contributing factors.

Although the input impedance  $Z'$  and the gain  $G'_0$  of the antenna should not change from scaling, changes have been observed, because the losses couldn't be scaled according to table 1. Conductivity and thickness of the aluminum were

left unchanged, because of the available process technology. The resistivity of the silicon wafer was changed to  $\rho = 10000 \Omega\text{cm}$ , a scaling factor of 10 instead of 12.5. Therefore, the scaling process will reduce the conductor losses and leave the dielectric losses at about the same amount.

The individual loss contributions of the scaled antenna have been computed to  $\eta_d = 0.89$ ,  $\eta_c = 0.89$  and  $\eta_s = 0.75$ . The overall efficiency is, therefore, somewhat higher than for the original antenna, at 60 % ( $\eta = 0.6$ ). As expected, the conductor losses decrease and the dielectric losses stay about the same. The surface wave losses remain unchanged.

## VII. CONCLUSION

A silicon based integrated patch antenna at an operating frequency of 122 GHz has been simulated, manufactured and measured. Far field pattern measurements have been performed with a scaled version of the antenna. It has been shown that the efficiency of the 122 GHz patch antenna is about 50%, leading to a gain of 3.2 dBi. The excitation of surface waves accounts for about 25% loss.

## VIII. ACKNOWLEDGEMENT

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